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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
JONES, ERIC W	

ART UNIT	PAPER NUMBER
2892	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/582,711	BLANCHARD, PIERRE	
	Examiner	Art Unit	
	ERIC W. JONES	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *1-15,24 and 26-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-23,25 and 30-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/8/2009 has been entered.

Allowable Subject Matter

2. The indicated allowability of claims 30-39 is withdrawn in view of the newly discovered reference(s) to Pourquier (WO 03/019669) as evidenced by Pourquier (US 6,960,483 B2-prior art of record) and Blanchard et al (US 6,621,107 B2) and Pourquier et al (WO 03/019668) as evidenced by Pourquier et al (US 7,217,590 B2-prior art of record). Rejections based on the newly cited reference(s) follow.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 16-21, 23, 25 and 30; 31-36, 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pourquier (WO 03/019669 hereafter Pourquier 669 (original and translation provided) as evidenced by Pourquier (US 6,960,483 B2 hereafter Pourquier 483-prior art of record) in view of Blanchard et al (US 6,621,107 B2).

Re claim 16, Pourquier 669 (as evidenced by Pourquier 483) discloses a process for the fabrication of electronic chips from a semiconductor wafer comprising, on its front face, a thin active layer of semiconductor material, the process comprising steps of:

formatting of etched layers (16 in FIG. 1) on the active layer (12 in FIG. 1); bonding the wafer (10 in FIG. 1) by its front face (FIG. 4) onto a support substrate (20 in FIG. 3); and thereafter thinning down of the semiconductor wafer via a backside (30 in FIG. 4) opposite the front face, depositing at least one metal layer (56 in FIG. 5) on the backside thus thinned,

said process including the following steps: etching trenches (25 in FIG. 2) into the thin active layer, before the bonding operation, these trenches extending into the wafer over a depth approximately equal to the residual semiconductor wafer thickness that will remain after the thinning operation (FIG. 4),

filling the space opened by said trenches with a conducting material (14 in FIG. 2) isolated (insulator 26 in FIG. 2) from the active layer (12), thus forming conducting vias between the front face and the backside of the thinned wafer (FIG. 4),

wherein said trenches comprise a series of trenches (FIG. 4) located under the contact pad (54 and 56 in FIG. 5), the contact pad being in electrical contact with the

conducting material in said parallel trenches. (Pourquier 483, column 3, lines 12-67; column 4, lines 1-37; column 5, lines 1-9)

Pourquier 669 fails to disclose etching at least one contact pad in said metal layer; and narrow, parallel, vertical trenches.

Blanchard et al disclose in FIGS. 5 and 6A-F narrow, parallel, vertical trenches (219a-c 0.4 to 2.0 microns in FIG. 5 and FIG. 6C; column 5, lines 48-55); and etching at least one contact pad in a metal layer (218 in FIGS 5 and 6F; column 8, lines 22-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the narrow, parallel, vertical trenches and etching at least one contact pad in a metal layer of Blanchard et al for the trenches and metal layer of Pourquier 669 to form trench-based semiconductor devices. (Blanchard et al, Title)

Re claim 17, Pourquier 669 (as evidenced by Pourquier 483) discloses the trenches are formed before other deposition and etching steps of electrically functional layers on the front face of the semiconductor wafer. (Pourquier 483, column 3, lines 32-62)

Re claim 18, Pourquier 669 fails to disclose the trench takes the form of an alignment marker visible from the backside after thinning in order to allow alignment of the patterns for etching of the layers on the backside with respect to the patterns for etching of layers on the front face.

The recitation 'the trench takes the form of an alignment marker visible from the backside after thinning in order to allow alignment of the patterns for etching of the layers on the backside with respect to the patterns for etching of layers on the front face'

is only a statement of the inherent properties of the 'process for the fabrication of electronic chips from a semiconductor wafer'. Once formed, the trenches can serve as alignment marks for subsequent backside device processing. The structure recited in Pourquier 669 is substantially identical to that of the claims, claimed properties or functions, therefore, are presumed to be similar. Or where the claimed and prior art products are produced by identical or substantially identical processes, a *prima facie* case of obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977). See MPEP § 2112.02.

Re claim 19, Pourquier 669 (as evidenced by Pourquier 483) discloses the metal layer (conductive boss 56 in FIG. 5) is deposited onto the backside of the wafer (30 in FIG. 5) after thinning, this layer being connected, by conducting vias (22 in FIG. 5) formed within at least one trench, to at least one conducting layer (22 in FIG. 5) formed. (Pourquier 483, column 3, lines 12-67; column 4, lines 1-37; column 5, lines 10-18)

Pourquier 669 (as evidenced by Pourquier 483) fails to disclose narrow trench; and prior to bonding the wafer onto the support substrate, on the front face of the wafer.

Blanchard et al disclose in FIGS. 5 and 6A-F narrow, parallel, vertical trenches (219a-c 0.4 to 2.0 microns in FIG. 5 and FIG. 6C; column 5, lines 48-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the narrow, parallel, vertical trenches of Blanchard et al as discussed above for claim 16.

With respect to prior to bonding the wafer onto the support substrate, it would have been obvious to one of ordinary skill in the art at the time the invention was made

to deposit said metal layer prior to bonding the wafer onto the support substrate since the selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results. *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946); *In re Gibson*, 39 F.2d 975, 5 USPQ 230 (CCPA 1930). See MPEP § 2144.04.

Re claim 20, Pourquier 669 (as evidenced by Pourquier 483) discloses said electronic chips comprise at least one image sensor with a matrix of pixels and the said at least one metal layer comprises a pattern within the matrix of pixels. (Pourquier 483, FIGS. 1 and 5; column 3, lines 9-26 and column 5, lines 10-18)

Re claim 21, Pourquier 669 (as evidenced by Pourquier 483) discloses layers of color filters are deposited onto the backside of the wafer after bonding and thinning. (Pourquier 483, column 5, lines 1-9)

Re claim 23, Pourquier (as evidenced by Pourquier 483) discloses the trenches (25 in FIG. 2) have their internal walls coated with an insulator (26 in FIG. 2) and are filled with a metal (14 in FIG. 2). (Pourquier 483, column 3, lines 54-62)

Pourquier 669 fails to disclose a thin silicon oxide and highly doped polycrystalline silicon.

Blanchard et al disclose in FIGS. 5 and 6A-F narrow, parallel, vertical trenches (219a-c 0.4 to 2.0 microns in FIG. 5 and FIG. 6C; column 5, lines 48-55) filled with silicon oxide (210 in FIGS. 5 and 6C; column 5, lines 60-67) and doped polysilicon (211 in FIGS. 5 and 6C; column 5, lines 60-67 and column 7, lines 51-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the narrow, parallel, vertical trenches with the silicon oxide and doped polysilicon fillings of Blanchard et al as discussed above for claims 16 and 19.

Re claim 25, Pourquier 669 fails to disclose the semiconductor wafer comprises a highly-doped silicon substrate coated with a more lightly doped epitaxial layer forming the active layer, of around 5 to 20 microns thickness, and in that the depth of the trenches is substantially equal to the thickness of the epitaxial layer.

Blanchard et al disclose in FIGS. 5 and 6A-c a semiconductor wafer comprises a highly-doped silicon substrate ($1x10^{19}$ to $5x10^{20}$ N^+-silicon 200 in FIG. 6A) coated with a more lightly doped epitaxial layer ($1x10^{15}$ to $5x10^{20}$ P-silicon 204 in FIG. 6A) forming the active layer, of around 0.3 to 5 microns thickness, and in that the depth of the trenches (219a-c in FIG. 5) is substantially equal (0.3 to 4 microns) to the thickness of the epitaxial layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the substrate doping level and the epitaxial layer doping level and thickness of Blanchard et al with the method of Pourquier 669 to form trench-based semiconductor devices. (Blanchard et al, Title)

Re claim 30, Pourquier 669 (as evidenced by Pourquier 483) discloses wherein said trenches (FIG. 5) comprise a continuous trench completely surrounding a semiconductor region (the trenches in FIG. 5 surround a region of semiconductive wafer 10) below said contact pad (56 in FIG. 5), the contact pad being electrically connected

through said semiconductor region to at least one conductive layer (metal 22 in FIG. 5) formed during said step of formatting. (Pourquier 483, column 3, lines 12-67; column 4, lines 1-37; column 5, lines 1-9)

Pourquier 669 fails to disclose a continuous trench completely surrounding said parallel trenches; and the contact pad being isolated from the conductive material filling said continuous trench.

Blanchard et al disclose in FIGS. 5 and 6A-F narrow, parallel, vertical trenches (219a-c 0.4 to 2.0 microns in FIG. 5 and FIG. 6C; column 5, lines 48-55); a continuous trench completely surrounding said parallel trenches (if FIGS. 5 and 6F were shown extended both right and left, a repeating series of trenches similar to 219a-c would obviously be seen; in which case those trenches would both completely surround said parallel trenches 219a-c and surround the semiconductor regions between the trenches); and the contact pad (218) being isolated (oxide 216 in FIG. 5; column 6, lines 43-49) from the conductive material filling (polysilicon 211 in FIG. 5; column 6, lines 43-49) said continuous trench.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the trench formation of Blanchard et al for the trenches of Pourquier 669, and to use them and the oxide isolation to form trench-based semiconductor devices. (Blanchard et al, Title)

Re claim 31, Pourquier 669 (as evidenced by Pourquier 483) discloses a process for the fabrication of contact pads of electronic chips in a semiconductor wafer

comprising, on a front face of the wafer, a thin active layer of semiconductor material, the process comprising steps of:

formatting of etched layers (16 in FIG. 1) on the active layer (12 in FIG. 1); bonding the wafer (10 in FIG. 1) by its front face (FIG. 4) onto a support substrate (20 in FIG. 3); and thereafter thinning down of the semiconductor wafer via a backside (30 in FIG. 4) opposite the front face, depositing at least one metal layer (56 in FIG. 5) on the backside thus thinned,

said process including the following steps: etching trenches (25 in FIG. 2) into the thin active layer, before the bonding operation, these trenches extending into the wafer over a depth approximately equal to the residual semiconductor wafer thickness that will remain after the thinning operation (FIG. 4),

filling the space opened by said trenches with a conducting material (14 in FIG. 2) isolated (insulator 26 in FIG. 2) from the active layer (12), thus forming conducting vias between the front face and the backside of the thinned wafer (FIG. 4),

wherein said trenches (FIG. 5) comprise a continuous trench completely surrounding a semiconductor region (the trenches in FIG. 5 surround a region of semiconductive wafer 10) below said contact pad (56 in FIG. 5), the contact pad being electrically connected through said semiconductor region to at least one conductive layer (metal 22 in FIG. 5) formed during said step of formatting. (Pourquier 483, column 3, lines 12-67; column 4, lines 1-37; column 5, lines 1-9)

Pourquier 669 fails to disclose etching at least one contact pad in said metal layer; narrow, parallel, vertical trenches; and the contact pad being isolated from the conductive material filling said continuous trench.

Blanchard et al disclose in FIGS. 5 and 6A-F narrow, parallel, vertical trenches (219a-c 0.4 to 2.0 microns in FIG. 5 and FIG. 6C; column 5, lines 48-55); etching at least one contact pad in a metal layer (218 in FIGS 5 and 6F; column 8, lines 22-35); and the contact pad (218) being isolated (oxide 216 in FIG. 5; column 6, lines 43-49) from the conductive material filling (polysilicon 211 in FIG. 5; column 6, lines 43-49) said continuous trench.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the narrow, parallel, vertical trenches and etching at least one contact pad in a metal layer of Blanchard et al for the trenches and metal layer of Pourquier 669, and to use them and the oxide isolation to form trench-based semiconductor devices. (Blanchard et al, Title)

Re claim 32, Pourquier 669 (as evidenced by Pourquier 483) discloses the trenches are formed before other deposition and etching steps of electrically functional layers on the front face of the semiconductor wafer. (Pourquier 483, column 3, lines 32-62)

Re claim 33, Pourquier 669 fails to disclose the trench takes the form of an alignment marker visible from the backside after thinning in order to allow alignment of the patterns for etching of the layers on the backside with respect to the patterns for etching of layers on the front face.

The recitation 'the trench takes the form of an alignment marker visible from the backside after thinning in order to allow alignment of the patterns for etching of the layers on the backside with respect to the patterns for etching of layers on the front face' is only a statement of the inherent properties of the 'process for the fabrication of electronic chips from a semiconductor wafer'. Once formed, the trenches can serve as alignment marks for subsequent backside device processing. The structure recited in Pourquier 669 is substantially identical to that of the claims, claimed properties or functions, therefore, are presumed to be similar. Or where the claimed and prior art products are produced by identical or substantially identical processes, a *prima facie* case of obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977). See MPEP § 2112.02.

Re claim 34, Pourquier 669 (as evidenced by Pourquier 483) discloses the metal layer (conductive boss 56 in FIG. 5) is deposited onto the backside of the wafer (30 in FIG. 5) after thinning, this layer being connected, by conducting vias (22 in FIG. 5) formed within at least one trench, to at least one conducting layer (22 in FIG. 5) formed. (Pourquier 483, column 3, lines 12-67; column 4, lines 1-37; column 5, lines 10-18)

Pourquier 669 (as evidenced by Pourquier 483) fails to disclose narrow trench; and prior to bonding the wafer onto the support substrate, on the front face of the wafer.

Blanchard et al disclose in FIGS. 5 and 6A-F narrow, parallel, vertical trenches (219a-c 0.4 to 2.0 microns in FIG. 5 and FIG. 6C; column 5, lines 48-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the narrow, parallel, vertical trenches of Blanchard et al as discussed above for claim 31.

With respect to prior to bonding the wafer onto the support substrate, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit said metal layer prior to bonding the wafer onto the support substrate since the selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results. *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946); *In re Gibson*, 39 F.2d 975, 5 USPQ 230 (CCPA 1930). See MPEP § 2144.04.

Re claim 35, Pourquier 669 (as evidenced by Pourquier 483) discloses said electronic chips comprise at least one image sensor with a matrix of pixels and the said at least one metal layer comprises a pattern within the matrix of pixels. (Pourquier 483, FIGS. 1 and 5; column 3, lines 9-26 and column 5, lines 10-18)

Re claim 36, Pourquier 669 (as evidenced by Pourquier 483) discloses layers of color filters are deposited onto the backside of the wafer after bonding and thinning. (Pourquier 483, column 5, lines 1-9)

Re claim 38, Pourquier (as evidenced by Pourquier 483) discloses the trenches (25 in FIG. 2) have their internal walls coated with an insulator (26 in FIG. 2) and are filled with a metal (14 in FIG. 2). (Pourquier 483, column 3, lines 54-62)

Pourquier 669 fails to disclose a thin silicon oxide and highly doped polycrystalline silicon.

Blanchard et al disclose in FIGS. 5 and 6A-F narrow, parallel, vertical trenches (219a-c 0.4 to 2.0 microns in FIG. 5 and FIG. 6C; column 5, lines 48-55) filled with silicon oxide (210 in FIGS. 5 and 6C; column 5, lines 60-67) and doped polysilicon (211 in FIGS. 5 and 6C; column 5, lines 60-67 and column 7, lines 51-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the narrow, parallel, vertical trenches with the silicon oxide and doped polysilicon fillings of Blanchard et al as discussed above for claims 16 and 19.

Re claim 39, Pourquier 669 fails to disclose the semiconductor wafer comprises a highly-doped silicon substrate coated with a more lightly doped epitaxial layer forming the active layer, of around 5 to 20 microns thickness, and in that the depth of the trenches is substantially equal to the thickness of the epitaxial layer.

Blanchard et al disclose in FIGS. 5 and 6A-c a semiconductor wafer comprises a highly-doped silicon substrate ($1x10^{19}$ to $5x10^{20}$ N^+-silicon 200 in FIG. 6A) coated with a more lightly doped epitaxial layer ($1x10^{15}$ to $5x10^{20}$ P-silicon 204 in FIG. 6A) forming the active layer, of around 0.3 to 5 microns thickness, and in that the depth of the trenches (219a-c in FIG. 5) is substantially equal (0.3 to 4 microns) to the thickness of the epitaxial layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the substrate doping level and the epitaxial layer doping level and thickness of Blanchard et al with the method of Pourquier 669 to form trench-based semiconductor devices. (Blanchard et al, Title)

6. Claims 22 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pourquier 669 (as evidenced by Pourquier 483) and Blanchard et al as applied to claims 16 and 31 above, and further in view of Pourquier et al (WO 03/019668 hereafter Pourquier 668 (original and translation provided) as evidenced by Pourquier (US 7,217,590 B2 hereafter Pourquier 590-prior art of record).

Re claims 22 and 37, Pourquier 669 and Blanchard et al fail to disclose the semiconductor wafer and its support substrate are bonded onto another, transparent, substrate and the support substrate is eliminated.

Pourquier 668 (as evidenced by Pourquier 590) disclose the semiconductor wafer (30 in FIG. 4) and its support substrate (20 in FIG. 4) are bonded onto another, transparent, substrate (80 in FIG. 7) and the support substrate is eliminated. (column 8, lines 33-62; column 9, lines 3-18)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the semiconductor wafer and its support substrate are bonded onto another, transparent, substrate and the support substrate is eliminated of Pourquier 668 (as evidenced by Pourquier 590) with the method of Pourquier 669 (as evidenced by Pourquier 483) and Blanchard et al to produce connection pads flush with the conductive layers of the imager. (Pourquier 590, column 9, lines 15-18)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC W. JONES whose telephone number is (571)270-3416. The examiner can normally be reached on Monday-Friday 5:30AM-3:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571)272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892

/ERIC W JONES/
Examiner, Art Unit 2892
8/13/2009